CA3040

Video and Wide-band Amplifier

For Industrial and Commercial
Equipment at Frequencies up to 200 MHz

Features:

- *High differential push-pull voltage gain - 37 dB typ.*
- *Single-ended voltage gain - 31 dB typ.*
- *Wide [3dB] bandwidth - 55 MHz typ.*
- *Balanced input and output*
- *High input resistance - 150 kΩ typ.*
- *Low output resistance - 125 Ω typ.*
- *Bias options for temperature compensation:*
  Bias Mode A: "Constant" Voltage
  Bias Mode B: "Constant" Gain

The RCA CA3040 is a monolithic silicon integrated circuit designed to meet the requirements of a wide variety of applications requiring high gain and wide bandwidth. The cascode-connected differential amplifier achieves a double-ended gain of 37 dB with a typical 3 dB bandwidth of 55 MHz. Emitter-Follower input and output stages provide the desirable high input impedance and output impedance for coupling to other circuits.

The CA3040 includes two biasing options, allowing the user to optimize his design over the entire military temperature range of −55 to +125° C. **Bias Mode A** yields a substantially constant voltage at the output terminals for applications using DC coupling to succeeding stages or requiring maximum dynamic range over the temperature range. DC output voltage varies less than 0.1 volt (typically) over the entire temperature range while gain varies ± 2 dB. **Bias Mode B** provides extremely stable gain over the temperature range. Gain variation is 0 dB (typically) in this Bias Mode. DC variation is ± 0.8 volt.

Provisions are also made for stabilizing the operating point for either single or split power supplies.

Applications

- *Video amplifier*
- *Schmitt trigger*
- *Modulator*
- *IF Amplifier*
- *Mixer*
- *DC Amplifier*
- *Sense Amplifier*

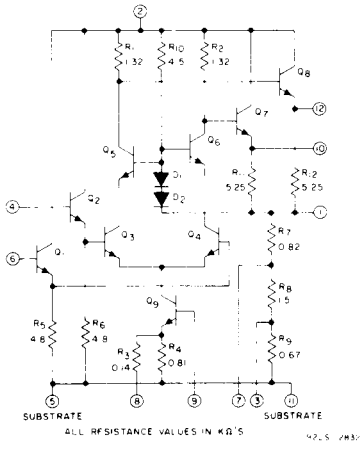


Fig. 1 — Schematic Diagram for CA3040.

The resistance values included on the schematic diagram have been supplied as a convenience to assist Equipment Manufacturers in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as ±30%.

RCA reserves the right to make any changes in the Resistance Values provided such changes do not adversely affect the published performance characteristics of the device.

File Number **363**

ABSOLUTE-MAXIMUM RATINGS

DISSIPATION * . . . . . 450 mW
Derating factor for $T_A > 85^oC$ . . . . . 5 mW/°C
TEMPERATURE RANGE:
Operating . . . . . -55°C to +125°C
Storage . . . . . -65°C to +150°C

LEAD TEMPERATURE (During Soldering):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. . . . . +265°C

* Limitation imposed by the thermal resistance of package.

MAXIMUM VOLTAGE RATINGS at $T_A = 25^oC$

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 2 with respect to terminal 11 is 0 to +14 volts.

TERMINAL No.	1	2	3	4	5▲	6	7	8	9	10	11▲	12
1		0 -14	*	*	+14 0	*	+10 -10	*	*	*	+14 0	*
2			*	+14 0	+14 0	+14 0	*	*	*	+14 0	+14 0	+14 0
3				*	+5 -3	*	*	*	*	*	+5 -3	*
4					*	+3 -3	*	*	*	*	*	*
5▲					▲	*	+10 -3	*	+3 -7	*	0 Note 1	*
6							*	*	*	*	*	*
7								*	*	*	+10 -3	*
8									+3 -3	*	*	*
9										*	+7 -3	*
10											*	*
11▲											▲	*
12												

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	5	5
2	-	-
3	5	5
4	1	0.1
5	-	-
6	1	0.1
7	5	5
8	5	5
9	1	0.1
10	-	10
11	-	-
12	-	10

▲ Reference Substrate

Note 1: External connection required for proper operation.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

CA3040

ELECTRICAL CHARACTERISTICS AT T_A = 25°C Unless Otherwise Specified

Characteristics	Symbols	Test Circuits Fig.	Special Test Conditions	Limits CA3040 Min.	Typ.	Max.	Units	Typical Characteristics Curves Fig.
STATIC CHARACTERISTICS	V_{CC} = +6V, V_{EE} = -6V							
Output Voltage	V_{10} or V_{12}	2(a) 2(b)	Bias Mode Switch A or B: Closed	1.4	2.7	3.7	V	9
Base Bias Voltage	V_9	2(a)	Bias Mode A Switch Closed	-	-1.7	-	V	-
		2(b)	Bias Mode B Switch Closed	-	-1.7	-	V	-
Input Bias Reference Voltage	V_1	2(a) 2(b)	Bias Mode Switch A or B: Open	-1	-	+1	V	9
Input Bias Current	I_4, I_6	2(a) 2(b)	Bias Mode Switch A or B: Closed	-	15	45	μA	-
Input Unbalance Current	$\lvert I_6 - I_4 \rvert$	2(a) 2(b)	Bias Mode Switch A or B: Closed	-	-	6	μA	-
Power Supply Current Drain	I_2 or $I_5 + I_{11}$	2(a)	Mode A Switch open or closed	4.7	8.5	15.5	mA	10
	I_2 or $I_5 + I_8 + I_{11}$	2(b)	Mode B Switch open or closed					
DYNAMIC CHARACTERISTICS	V_{CC} = +12V, V_{EE} = 0, Split Voltage Supply (Optional) = +6V							
Differential Voltage Gain								-
Single-Ended Input Differential Output	$A_{DIFF(DE)}$	3(a)	f = 1 MHz R_S = 50 Ω	34	37	-	dB	-
Single-Ended Input and Output	$A_{DIFF(SE)}$	3(a)	f = 1 MHz R_S = 50 Ω	28	31	-	dB	4,5
-3 dB Bandwidth	BW	3(a)	R_S = 50 Ω	40	55	-	MHz	4,7
Differential Voltage Gain Balance	$A_{DIFF(SE)10} - A_{DIFF(SE)12}$	3(a)	f = 1 MHz	-1	0	+1	dB	-
Output Voltage Swing	V_8 or V_{10} RMS	3(a)	f = 1 MHz R_S = 50 Ω	-	0.5	-	V_{RMS}	7
Noise Figure	NF	3(a)	(Note 1) f = 30 MHz R_S = 400 Ω	-	7.5	9	dB	8
Parallel Input Resistance	R_I	3(a)	f = 1 MHz	-	150	-	kΩ	-
Parallel Input Capacitance	C_I	3(a)		-	2.2	-	pF	-
Output Resistance	R_O	3(a)		-	125	-	Ω	-
TEMPERATURE DEPENDENT CHARACTERISTICS Temperature coefficients for ambient temperature: -55°C ≤ T_A ≤ +125°C								
Output Voltage	$\frac{\Delta V_{10} \text{ or } \Delta V_{12}}{^\circ C}$	3(a)	Bias Mode A	-	0	-	mV/°C	9
		3(b)	Bias Mode B	-	6.4	-	mV/°C	
Power Supply Current Drain	$\Delta I_2/^\circ C$	3(a)	Bias Mode A	-	5	-	μA/°C	11
Differential Voltage Gain	$A_{DIFF}/^\circ C$	3(a)	Bias Mode A	-	0.0166	-	dB/°C	12
		3(b)	Bias Mode B	-	0	-		

Note 1: Replace 1-kΩ resistors between Term. 1 and 4 and Term. 1 and 6 with suitable chokes so that reactance at 30 MH_Z exceeds 5kΩ

STATIC CHARACTERISTICS TEST CIRCUITS FOR CA3040

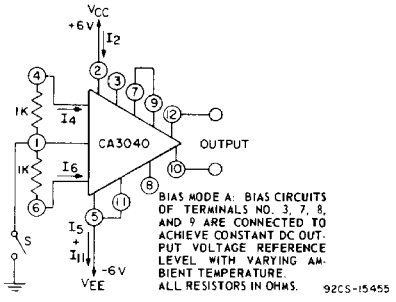


Fig.2(a) - Bias Mode A

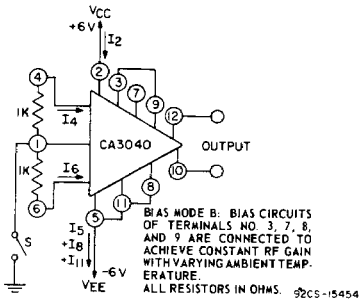
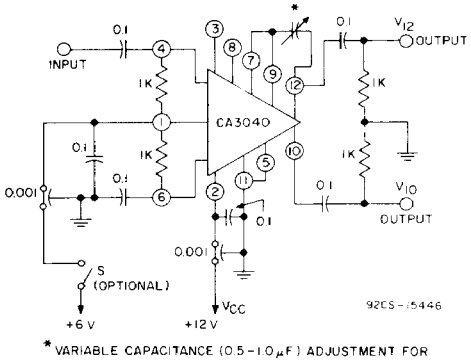


Fig.2(b) - Bias Mode B

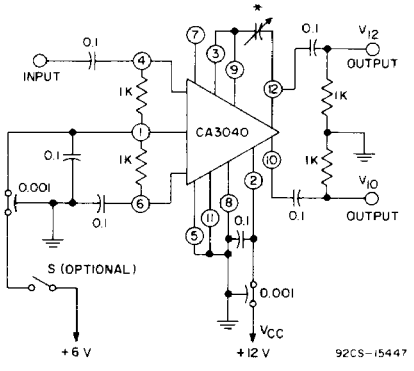
DYNAMIC CHARACTERISTICS TEST CIRCUITS FOR CA3040



* VARIABLE CAPACITANCE (0.5 - 1.0 μF) ADJUSTMENT FOR EQUAL 3dB BANDWIDTH AT AMPLIFIER OUTPUTS, TERMINALS 10 AND 12.

ALL RESISTORS IN OHMS.
ALL CAPACITORS IN MICROFARADS (UNLESS OTHERWISE INDICATED).
BIAS MODE A IS AS DEFINED IN FIG. 2 (a)

Fig.3(a) - Bias Mode A



* SEE FIG 3(a)
BIAS MODE B IS AS DEFINED IN FIG 2(b)
ALL RESISTORS IN OHMS.
ALL CAPACITORS IN MICROFARADS (UNLESS OTHERWISE INDICATED).

Fig.3(b) - Bias Mode B

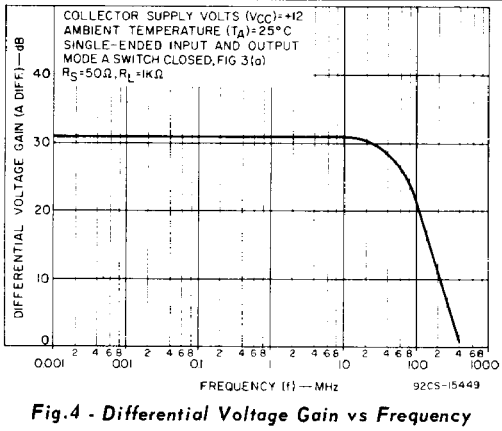


Fig.4 - Differential Voltage Gain vs Frequency

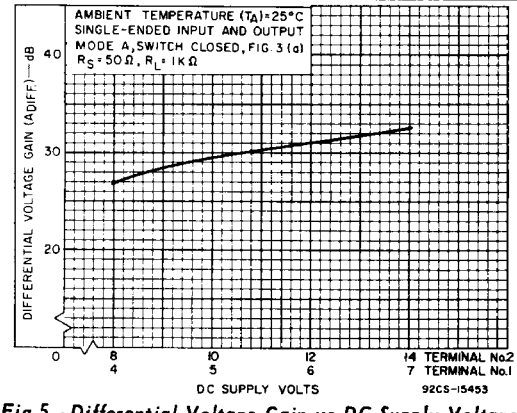


Fig.5 - Differential Voltage Gain vs DC Supply Voltages

OPERATING CONSIDERATIONS

General

The CA3040 is designed to provide flexibility in the selection of power supply configurations and to provide the circuit designer the choice between two modes of temperature-compensated performance. Mode A, which provides constant DC output voltage, is recommended for most applications. The control of the operating point provided by this mode maintains the dynamic range of the device while gain variation over most of the range is less than ±1 dB. Mode B provides constant gain for applications where this consideration is critical, but will exhibit a reduction of dynamic range at the temperature extremes.

Power Supply Considerations

Figures 2 and 3 illustrate the use of the CA3040 with balanced dual supplies and single power supplies, respectively. Both figures demonstrate that the inputs may be directly referenced to the center point of the supply (ground in Fig.2) by closing the included switch. This is the natural connection in Fig.2. This connection is optional, however, and need not be made. Use of this connection in Fig.3 implies the presence of another DC supply or a "stiff" bleeder. If such a source is present its use is suggested in order to maintain maximum common mode range. Dynamic performance and dynamic range of the output circuit are unaffected by the choice of biasing scheme used so that in most cases direct connection of Terminal No.1 to the center point of the supply is not required. Where direct connection is not used, Terminals No.4 and No.6 must be biased from Terminal No.1 for proper operation.

High-Frequency Considerations

Stable high-frequency operation requires that proper high-frequency construction techniques be followed. The photograph of Fig.6 illustrates the precautions taken in the construction of the test circuit of Fig.3.

Extreme caution is required because of the extended gain bandwidth capability of the device. Oscillations have been observed in the 400-to-800 MHz range when precautions were not taken. In addition to normal considerations of shielding, parts layout, and isolation, the following specific suggestions are made:

1. Use sockets only when necessary. Sockets, when used, must provide shielding within the pin circle. The socket shown in the chassis of Fig.6 is a Barnes MG-1201, or equivalent, modified by drilling a 1/8" hole in the center and inserting a grounded brass pin.
2. Do not bypass Terminal No.9 in normal operation. Fig.3 shows the use of neutralization between Terminal No.9 and one output to balance the amplifier at high frequencies. Experience shows that stable operation, while possible, is difficult to achieve if Terminal No.9 is bypassed to ground.
3. In DC testing, 1 kΩ, 1/4 W carbon resistors should be soldered directly to the socket Terminals No.4 and No.6 to suppress parasitic oscillations. All current carrying connections are made at the other end of the resistors. Direct sensing of Terminal No.4 or No.6 voltage should not be attempted.

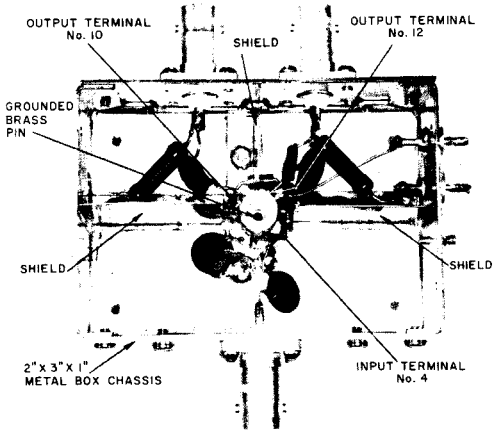


Fig.6 - Test Circuit Layout

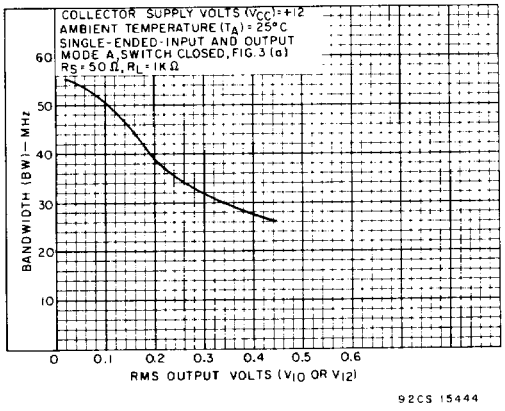


Fig.7 - 3dB Bandwidth vs Single-Ended Output Voltage

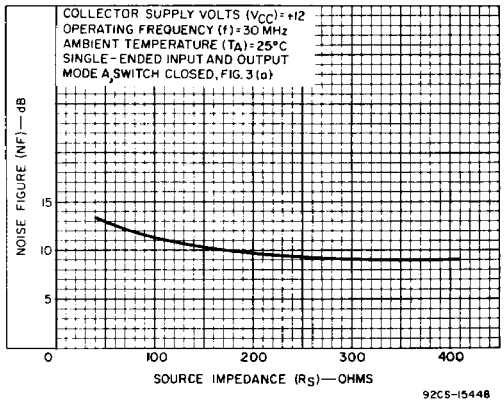


Fig.8 - Noise Figure (NF) vs Source Impedance

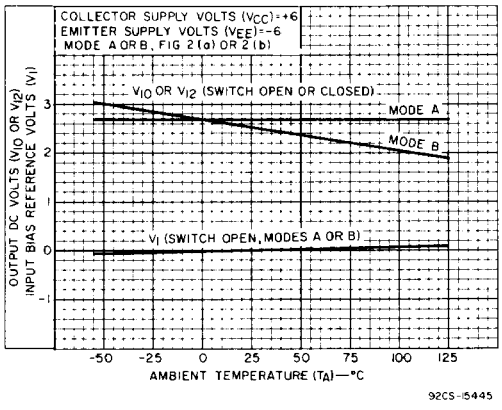


Fig.9 - Output Volts or Input Bias Reference Volts vs Ambient Temperature

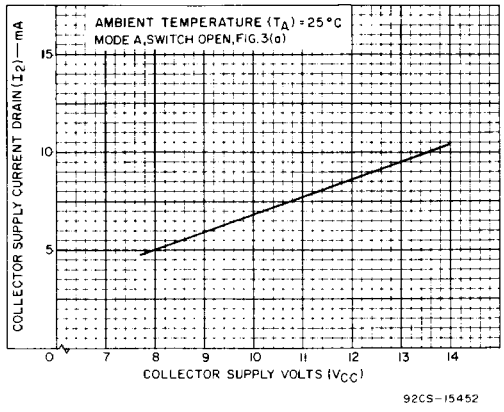


Fig.10 - Collector Supply Current Drain (I_2) vs Collector Supply Voltage (V_{CC})

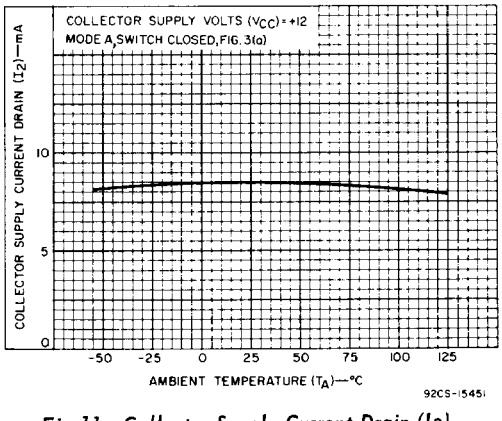


Fig.11 - Collector Supply Current Drain (I_2) vs Ambient Temperature

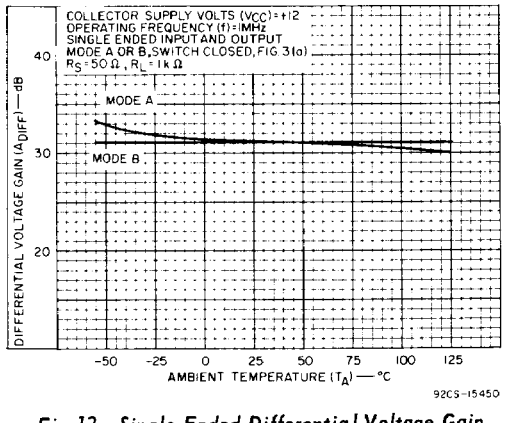


Fig.12 - Single-Ended Differential Voltage Gain vs Ambient Temperature